

TPS1100, TPS1100Y SINGLE P-CHANNEL ENHANCEMENT-MODE MOSFETS

SLVS078C – DECEMBER 1993 – REVISED AUGUST 1995

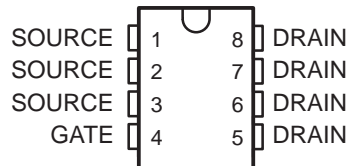
- Low $r_{DS(on)}$. . . 0.18 Ω Typ at $V_{GS} = -10$ V
- 3 V Compatible
- Requires No External V_{CC}
- TTL and CMOS Compatible Inputs
- $V_{GS(th)} = -1.5$ V Max
- Available in Ultrathin TSSOP Package (PW)
- ESD Protection Up to 2 kV Per MIL-STD-883C, Method 3015

description

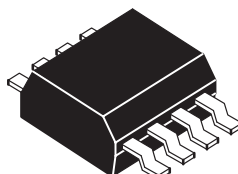
The TPS1100 is a single P-channel enhancement-mode MOSFET. The device has been optimized for 3-V or 5-V power distribution in battery-powered systems by means of Texas Instruments LinBiCMOS™ process. With a maximum $V_{GS(th)}$ of -1.5 V and an I_{DSS} of only 0.5 μ A, the TPS1100 is the ideal high-side switch for low-voltage, portable battery-management systems where maximizing battery life is a primary concern. The low $r_{DS(on)}$ and excellent ac characteristics (rise time 10 ns typical) make the TPS1100 the logical choice for low-voltage switching applications such as power switches for pulse-width-modulated (PWM) controllers or motor/bridge drivers.

The ultrathin thin shrink small-outline package or TSSOP (PW) version with its smaller footprint and reduction in height fits in places where other P-channel MOSFETs cannot. The size advantage is especially important where board real estate is at a premium and height restrictions do not allow for a small-outline integrated circuit (SOIC) package.

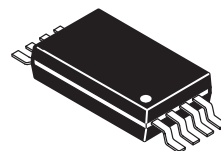
D OR PW PACKAGE
(TOP VIEW)



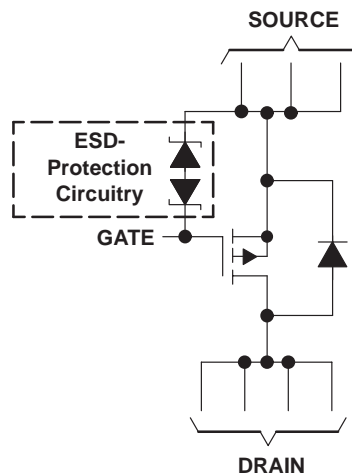
D PACKAGE



PW PACKAGE



schematic



NOTE A: For all applications, all source pins should be connected and all drain pins should be connected.

AVAILABLE OPTIONS

T _A	PACKAGED DEVICES		CHIP FORM (Y)
	SMALL OUTLINE (D)	PLASTIC DIP (P)	
-40°C to 85°C	TPS1100D	TPS1100PWLE	TPS1100Y

The D package is available taped and reeled. Add an R suffix to device type (e.g., TPS1100DR). The PW package is available only left-end taped and reeled (indicated by the LE suffix on the device type; e.g., TPS1100PWLE). The chip form is tested at 25°C.



Caution. This device contains circuits to protect its inputs and outputs against damage due to high static voltages or electrostatic fields. These circuits have been qualified to protect this device against electrostatic discharges (ESD) of up to 2 kV according to MIL-STD-883C, Method 3015; however, it is advised that precautions be taken to avoid application of any voltage higher than maximum-rated voltages to these high-impedance circuits.

LinBiCMOS is a trademark of Texas Instruments Incorporated.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 1995, Texas Instruments Incorporated

TPS1100, TPS1100Y SINGLE P-CHANNEL ENHANCEMENT-MODE MOSFETS

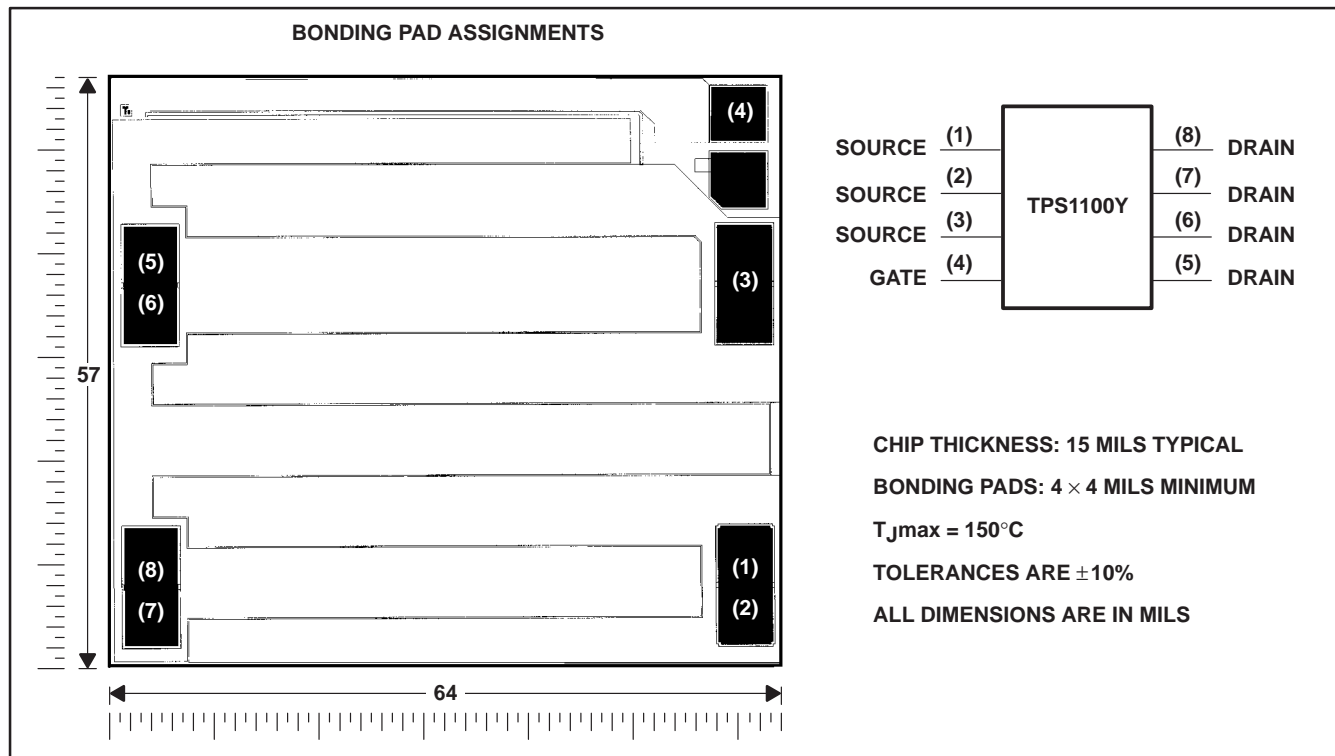
SLVS078C – DECEMBER 1993 – REVISED AUGUST 1995

description (continued)

Such applications include notebook computers, personal digital assistants (PDAs), cellular telephones, and PCMCIA cards. For existing designs, the D-packaged version has a pinout common with other p-channel MOSFETs in SOIC packages.

TPS1100Y chip information

This chip, when properly assembled, displays characteristics similar to the TPS1100. Thermal compression or ultrasonic bonding may be used on the doped aluminum bonding pads. The chips may be mounted with conductive epoxy or a gold-silicon preform.



TPS1100, TPS1100Y

SINGLE P-CHANNEL ENHANCEMENT-MODE MOSFETS

SLVS078C – DECEMBER 1993 – REVISED AUGUST 1995

absolute maximum ratings over operating free-air temperature (unless otherwise noted)[†]

				UNIT	
Drain-to-source voltage, V_{DS}				-15	V
Gate-to-source voltage, V_{GS}				2 or -15	V
Continuous drain current ($T_J = 150^\circ\text{C}$), I_D^\ddagger	$V_{GS} = -2.7\text{ V}$	D package	$T_A = 25^\circ\text{C}$	± 0.41	A
			$T_A = 125^\circ\text{C}$	± 0.28	
		PW package	$T_A = 25^\circ\text{C}$	± 0.4	
			$T_A = 125^\circ\text{C}$	± 0.23	
	$V_{GS} = -3\text{ V}$	D package	$T_A = 25^\circ\text{C}$	± 0.6	
			$T_A = 125^\circ\text{C}$	± 0.33	
		PW package	$T_A = 25^\circ\text{C}$	± 0.53	
			$T_A = 125^\circ\text{C}$	± 0.27	
	$V_{GS} = -4.5\text{ V}$	D package	$T_A = 25^\circ\text{C}$	± 1	
			$T_A = 125^\circ\text{C}$	± 0.47	
		PW package	$T_A = 25^\circ\text{C}$	± 0.81	
			$T_A = 125^\circ\text{C}$	± 0.37	
$V_{GS} = -10\text{ V}$	D package	$T_A = 25^\circ\text{C}$	± 1.6		
		$T_A = 125^\circ\text{C}$	± 0.72		
	PW package	$T_A = 25^\circ\text{C}$	± 1.27		
		$T_A = 125^\circ\text{C}$	± 0.58		
Pulsed drain current, I_D^\ddagger			$T_A = 25^\circ\text{C}$	± 7	A
Continuous source current (diode conduction), I_S			$T_A = 25^\circ\text{C}$	-1	A
Storage temperature range, T_{stg}				-55 to 150	$^\circ\text{C}$
Operating junction temperature range, T_J				-40 to 150	$^\circ\text{C}$
Operating free-air temperature range, T_A				-40 to 125	$^\circ\text{C}$
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds				260	$^\circ\text{C}$

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

[‡] Maximum values are calculated using a derating factor based on $R_{\theta JA} = 158^\circ\text{C}/\text{W}$ for the D package and $R_{\theta JA} = 248^\circ\text{C}/\text{W}$ for the PW package. These devices are mounted on a FR4 board with no special thermal considerations.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR [‡] ABOVE $T_A = 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$ POWER RATING	$T_A = 85^\circ\text{C}$ POWER RATING	$T_A = 125^\circ\text{C}$ POWER RATING
D	791 mW	6.33 mW/ $^\circ\text{C}$	506 mW	411 mW	158 mW
PW	504 mW	4.03 mW/ $^\circ\text{C}$	323 mW	262 mW	101 mW

[‡] Maximum values are calculated using a derating factor based on $R_{\theta JA} = 158^\circ\text{C}/\text{W}$ for the D package and $R_{\theta JA} = 248^\circ\text{C}/\text{W}$ for the PW package. These devices are mounted on an FR4 board with no special thermal considerations when tested.

TPS1100, TPS1100Y SINGLE P-CHANNEL ENHANCEMENT-MODE MOSFETS

SLVS078C – DECEMBER 1993 – REVISED AUGUST 1995

electrical characteristics at $T_J = 25^\circ\text{C}$ (unless otherwise noted)

static

PARAMETER	TEST CONDITIONS	TPS1100			TPS1100Y			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
$V_{GS(th)}$ Gate-to-source threshold voltage	$V_{DS} = V_{GS}, I_D = -250 \mu\text{A}$	-1	-1.25	-1.50	-1.25			V
V_{SD} Source-to-drain voltage (diode-forward voltage) [†]	$I_S = -1 \text{ A}, V_{GS} = 0 \text{ V}$		-0.9		-0.9			V
I_{GSS} Reverse gate current, drain short circuited to source	$V_{DS} = 0 \text{ V}, V_{GS} = -12 \text{ V}$			± 100				nA
I_{DSS} Zero-gate-voltage drain current	$V_{DS} = -12 \text{ V}, V_{GS} = 0 \text{ V}$	$T_J = 25^\circ\text{C}$		-0.5				μA
		$T_J = 125^\circ\text{C}$		-10				
$r_{DS(on)}$ Static drain-to-source on-state resistance [†]	$V_{GS} = -10 \text{ V}, I_D = -1.5 \text{ A}$		180		180			m Ω
	$V_{GS} = -4.5 \text{ V}, I_D = -0.5 \text{ A}$		291	400	291			
	$V_{GS} = -3 \text{ V}, I_D = -0.2 \text{ A}$		476	700	476			
	$V_{GS} = -2.7 \text{ V}, I_D = -0.2 \text{ A}$		606	850	606			
g_{fs} Forward transconductance [†]	$V_{DS} = -10 \text{ V}, I_D = -2 \text{ A}$		2.5		2.5			S

[†] Pulse test: pulse duration $\leq 300 \mu\text{s}$, duty cycle $\leq 2\%$

dynamic

PARAMETER	TEST CONDITIONS	TPS1100, TPS1100Y			UNIT
		MIN	TYP	MAX	
Q_g Total gate charge	$V_{DS} = -10 \text{ V}, V_{GS} = -10 \text{ V}, I_D = -1 \text{ A}$		5.45		nC
Q_{gs} Gate-to-source charge			0.87		
Q_{gd} Gate-to-drain charge			1.4		
$t_{d(on)}$ Turn-on delay time	$V_{DD} = -10 \text{ V}, R_L = 10 \Omega, I_D = -1 \text{ A}, R_G = 6 \Omega,$ See Figures 1 and 2		4.5		ns
$t_{d(off)}$ Turn-off delay time			13		ns
t_r Rise time			10		ns
t_f Fall time			2		
$t_{rr(SD)}$ Source-to-drain reverse recovery time		$I_F = 5.3 \text{ A}, di/dt = 100 \text{ A}/\mu\text{s}$		16	



PARAMETER MEASUREMENT INFORMATION

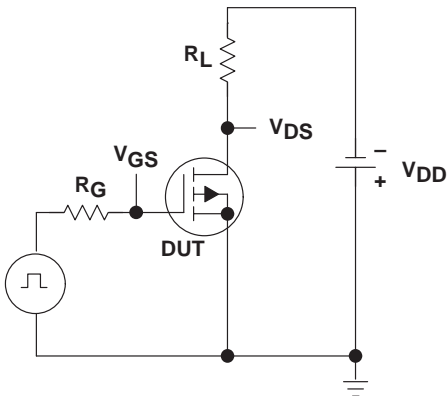


Figure 1. Switching-Time Test Circuit

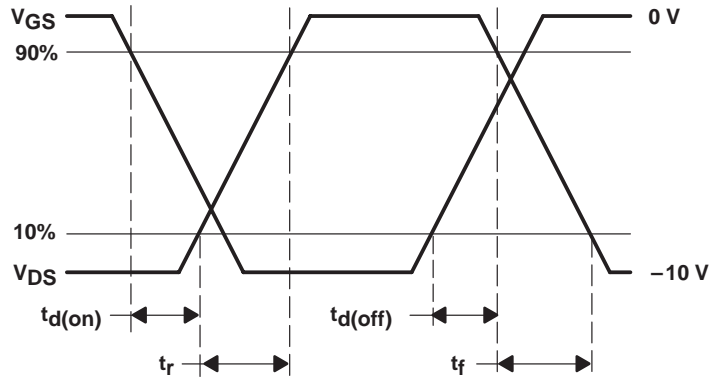


Figure 2. Switching-Time Waveforms

TYPICAL CHARACTERISTICS

Table of Graphs

		FIGURE
Drain current	vs Drain-to-source voltage	3
Drain current	vs Gate-to-source voltage	4
Static drain-to-source on-state resistance	vs Drain current	5
Capacitance	vs Drain-to-source voltage	6
Static drain-to-source on-state resistance (normalized)	vs Junction temperature	7
Source-to-drain diode current	vs Source-to-drain voltage	8
Static drain-to-source on-state resistance	vs Gate-to-source voltage	9
Gate-to-source threshold voltage	vs Junction temperature	10
Gate-to-source voltage	vs Gate charge	11

TPS1100, TPS1100Y SINGLE P-CHANNEL ENHANCEMENT-MODE MOSFETS

SLVS078C – DECEMBER 1993 – REVISED AUGUST 1995

TYPICAL CHARACTERISTICS

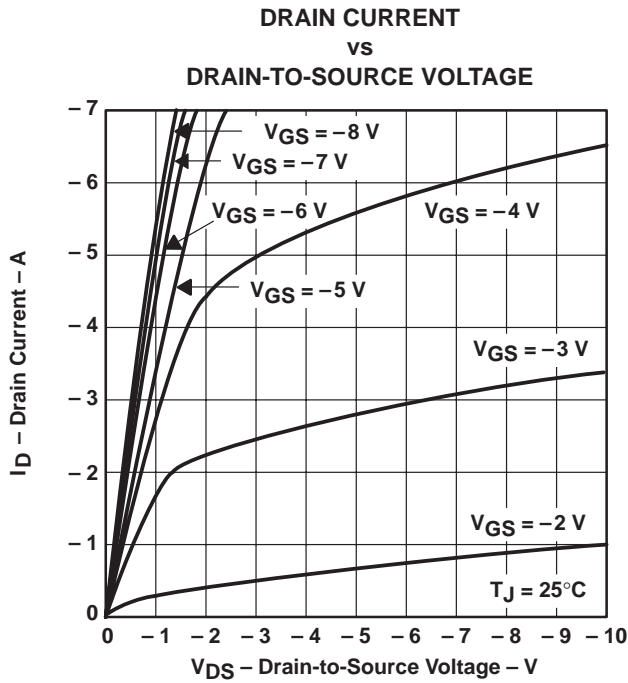


Figure 3

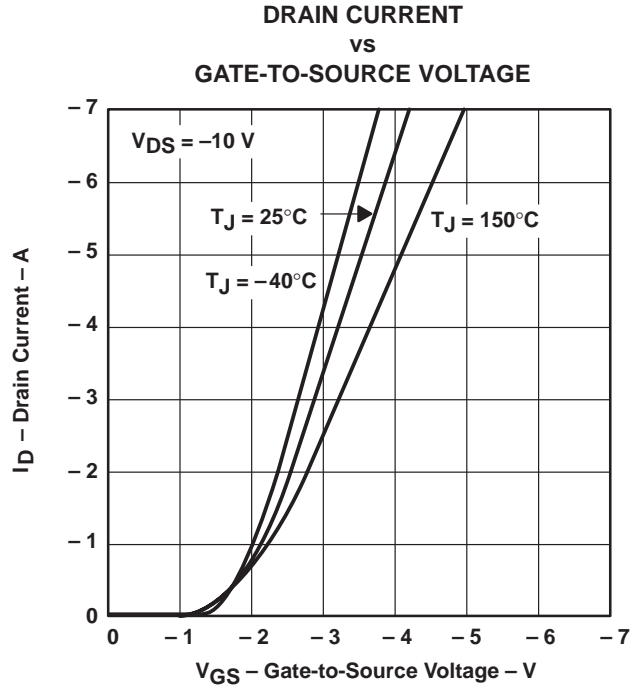


Figure 4

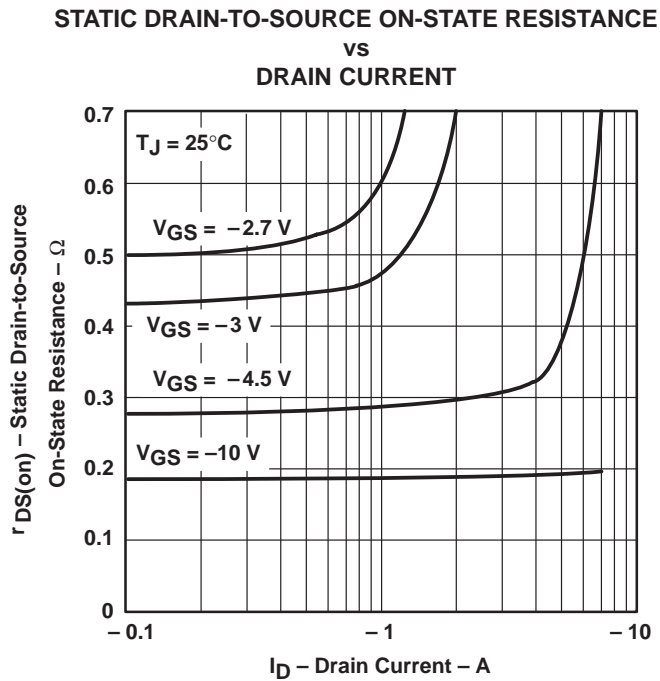


Figure 5

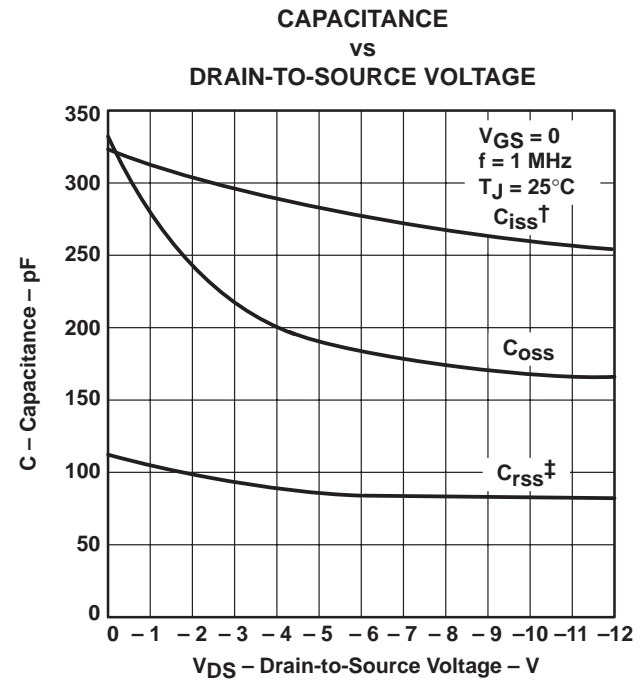


Figure 6

$$\dagger C_{iss} = C_{gs} + C_{gd} \cdot C_{ds(\text{shorted})}$$

$$\ddagger C_{rss} = C_{gd} \cdot C_{oss} = C_{ds} + \frac{C_{gs} C_{gd}}{C_{gs} + C_{gd}} \approx C_{ds} + C_{gd}$$



TYPICAL CHARACTERISTICS

STATIC DRAIN-TO-SOURCE
ON-STATE RESISTANCE (NORMALIZED)
vs
JUNCTION TEMPERATURE

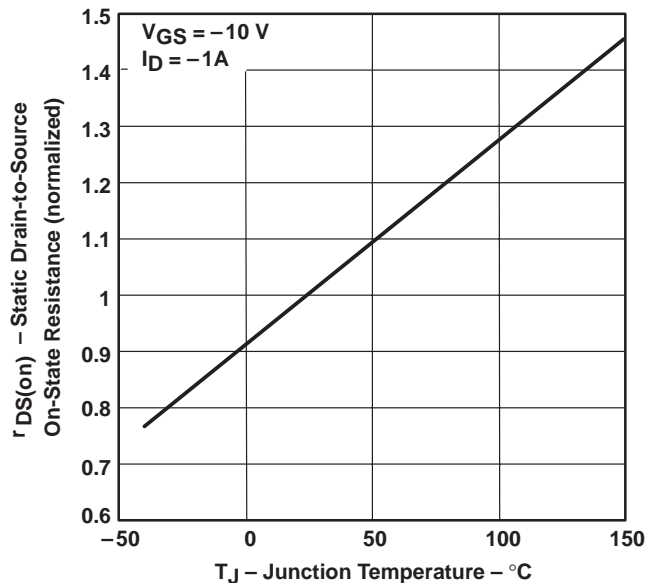


Figure 7

SOURCE-TO-DRAIN DIODE CURRENT
vs
SOURCE-TO-DRAIN VOLTAGE

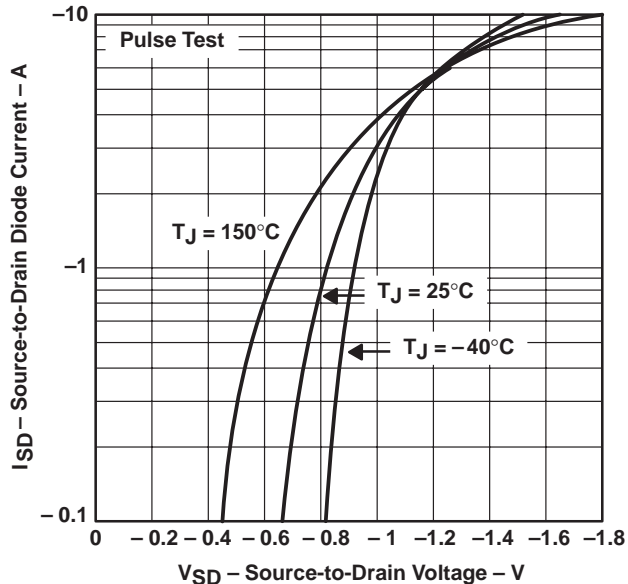


Figure 8

STATIC DRAIN-TO-SOURCE ON-STATE RESISTANCE
vs
GATE-TO-SOURCE VOLTAGE

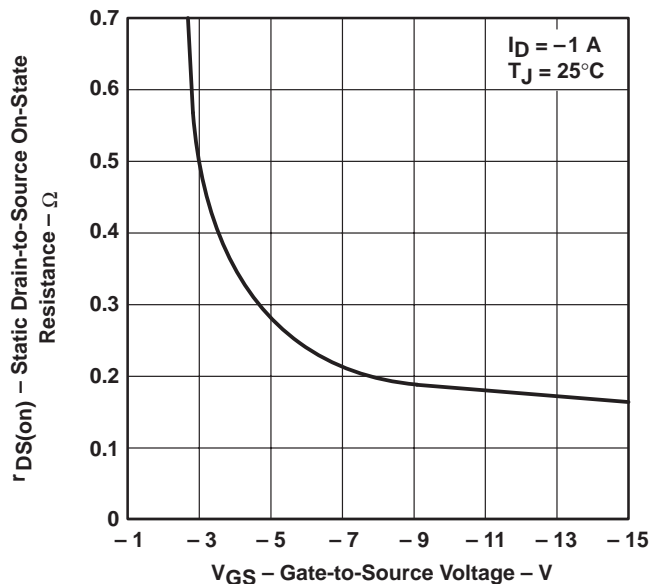


Figure 9

GATE-TO-SOURCE THRESHOLD VOLTAGE
vs
JUNCTION TEMPERATURE

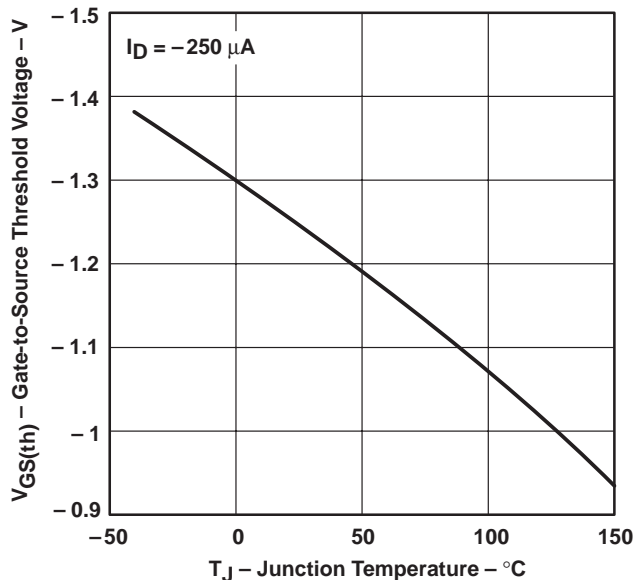


Figure 10

TPS1100, TPS1100Y SINGLE P-CHANNEL ENHANCEMENT-MODE MOSFETS

SLVS078C – DECEMBER 1993 – REVISED AUGUST 1995

TYPICAL CHARACTERISTICS

GATE-TO-SOURCE VOLTAGE
vs
GATE CHARGE

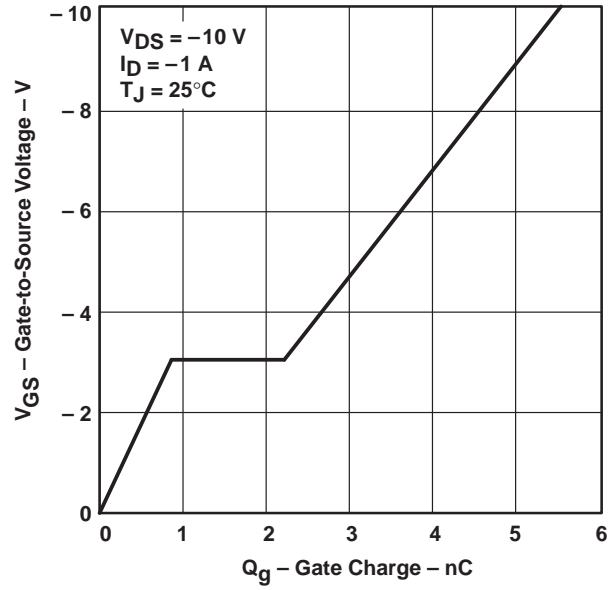
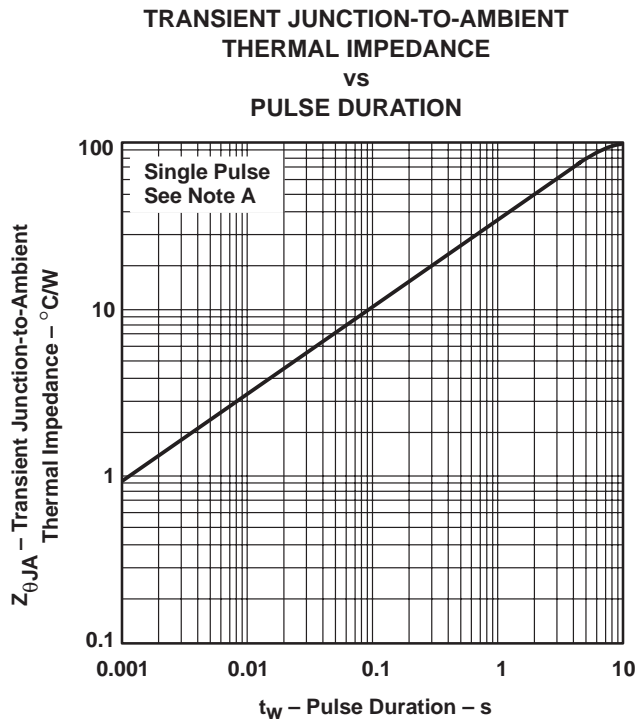
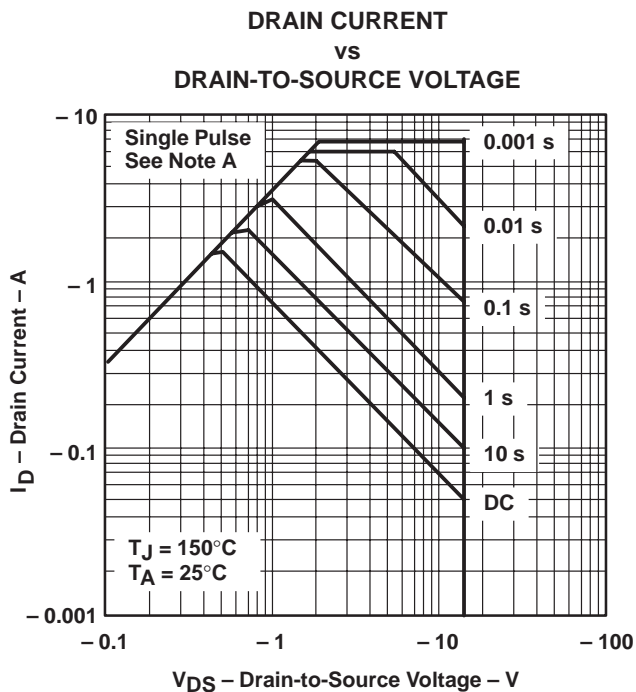


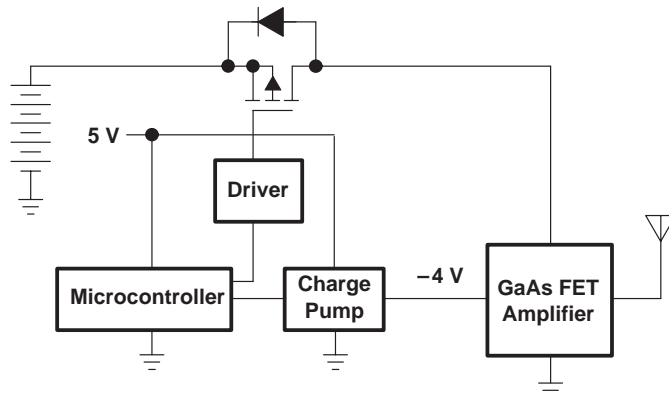
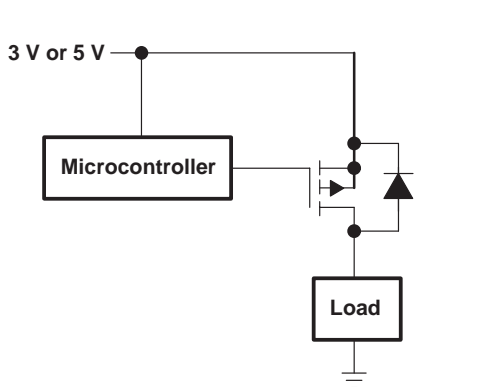
Figure 11

THERMAL INFORMATION



NOTE A: Values are for the D package and are FR4-board mounted only.

APPLICATION INFORMATION



PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
TPS1100D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		1100	Samples
TPS1100DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		1100	Samples
TPS1100DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		1100	Samples
TPS1100DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		1100	Samples
TPS1100PW	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		PS1100	Samples
TPS1100PWG4	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		PS1100	Samples
TPS1100PWLE	OBSOLETE	TSSOP	PW	8		TBD	Call TI	Call TI			
TPS1100PWR	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		PS1100	Samples
TPS1100PWRG4	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		PS1100	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ Only one of markings shown within the brackets will appear on the physical device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS1100DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TPS1100PWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS1100DR	SOIC	D	8	2500	340.5	338.1	20.6
TPS1100PWR	TSSOP	PW	8	2000	367.0	367.0	35.0

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as "components") are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI's terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers' products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers' products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI's goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have **not** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products

Audio	www.ti.com/audio
Amplifiers	amplifier.ti.com
Data Converters	dataconverter.ti.com
DLP® Products	www.dlp.com
DSP	dsp.ti.com
Clocks and Timers	www.ti.com/clocks
Interface	interface.ti.com
Logic	logic.ti.com
Power Mgmt	power.ti.com
Microcontrollers	microcontroller.ti.com
RFID	www.ti-rfid.com
OMAP Applications Processors	www.ti.com/omap
Wireless Connectivity	www.ti.com/wirelessconnectivity

Applications

Automotive and Transportation	www.ti.com/automotive
Communications and Telecom	www.ti.com/communications
Computers and Peripherals	www.ti.com/computers
Consumer Electronics	www.ti.com/consumer-apps
Energy and Lighting	www.ti.com/energy
Industrial	www.ti.com/industrial
Medical	www.ti.com/medical
Security	www.ti.com/security
Space, Avionics and Defense	www.ti.com/space-avionics-defense
Video and Imaging	www.ti.com/video

TI E2E Community

e2e.ti.com